

## Claims

- 1 1. An FET comprising:  
2 a gate having a top and bottom portion, the top portion having a width that is greater  
3 than the width of the bottom portion; and  
4 a diffusion self-aligned to the bottom portion.
- 1 2. The FET as recited in claim 1, wherein said diffusion comprises a first implant.
- 1 3. The FET as recited in claim 2, wherein said first implant comprises a halo implant.
- 1 4. The FET as recited in claim 2, wherein said first implant is directed at an angle from  
2 the normal to provide said implant self-aligned to said bottom portion.
- 1 5. The FET as recited in claim 1, further comprising a second implant defined by said  
2 top portion.
- 1 6. The FET as recited in claim 5, wherein said second implant comprises an extension  
2 implant.
- 1 7. The FET as recited in claim 1, further comprising a spacer adjacent said top portion  
2 and a third implant defined by said spacer.
- 1 8. The FET as recited in claim 7, wherein said third implant comprises a source/drain  
2 implant.

1 9. An FET comprising a gate, said gate comprising first conductive material and a  
2 second conductive material different from said first conductive material, said second  
3 conductive material on said first conductive material, wherein said second conductive  
4 material extends beyond said first conductive material to provide a T-shaped gate.

Q4 1 10. The FET of claim 9, wherein said first conductive material is on a gate dielectric and  
2 said gate dielectric is on a substrate.

1 11. The FET of claim 9, wherein said first material has a dimension less than a  
2 photolithographic minimum dimension.

1 12. The FET of claim 9, wherein said first material comprises a first semiconductor  
2 material.

1 13. The FET of claim 12, wherein said first semiconductor material comprises  
2 germanium.

1 14. The FET of claim 12, wherein said first semiconductor material comprises a  
2 germanium compound  $\text{Ge}_x\text{Si}_{1-x}$ , wherein x is in the range of about 0.5 to about 1.0.

Q5 1 15. The FET of claim 9, wherein said second conductive material comprises polysilicon.

1 16. The FET of claim 9, wherein said first conductive material comprises polysilicon.

1 17. The FET of claim 16, wherein said second conductive material comprises a refractory  
2 metal.

1 18. The FET of claim 17, wherein said second conductive material comprises tungsten,  
2 tantalum, molybdenum, or titanium.

1 19. The FET of claim 9, wherein said second conductive material comprises a silicide.

1 20. The FET of claim 9, further comprising a spacer along sidewalls of said second  
2 conductive material.

1 21. The FET of claim 13, wherein an air gap is left behind said spacer along a notched  
2 sidewall of said first conductive material.

1 22. A method of fabricating a semiconductor device comprising the steps of:  
2 providing a substrate formed of a first material, said substrate having a surface;  
3 forming a gate dielectric on said surface;  
4 forming a gate conductor on said gate dielectric;  
5 chemically reacting edges of said gate conductor adjacent said gate dielectric to  
6 form a first reaction product; and  
7 selectively removing said first reaction product with respect to remaining portions  
8 of said gate conductor so as to provide a notch in said gate conductor.

1 23. The method as recited in claim 22, wherein the step of forming a gate conductor  
2 comprises a first gate layer and a second gate layer, wherein said first gate layer  
3 contacts said gate dielectric and said second gate layer is on said first gate layer.

1 24. The method as recited in claim 23, wherein the step of chemically reacting edges of  
2 said first gate layer forms said first reaction product.

1 25. The method as recited in claim 24, wherein the step of selectively removing said first  
2 reaction product further includes removing said first reaction product with respect to  
3 remaining portions of said first gate layer and said second gate layer so as to provide a  
4 notch in said first gate layer.

1 26. The method as recited in claim 22, further comprising providing a spacer along  
2 sidewalls of said second gate layer.

1 27. The method as recited in claim 26, wherein an air gap is left behind said spacer along  
2 sidewalls of said first gate layer.

1 28. The method as recited in claim 22, wherein said first gate layer comprises germanium.

1 29. The method as recited in claim 22, wherein said first gate layer comprises a  
2 germanium compound  $\text{Ge}_x\text{Si}_{1-x}$ , wherein x is in the range of about 0.5 to about 1.0.

1 30. The method as recited in claim 22, wherein said second gate layer comprises silicon.

1 31. The method as recited in claim 22, wherein in said first reaction product comprises  
2 germanium oxide, or silicon germanium oxide.

1 32. The method as recited in claim 22, wherein said first gate layer comprises silicon.

1 33. The method as recited in claim 32, wherein said second gate layer comprises a  
2 refractory metal.

1 34. The method as recited in claim 33, wherein said second gate layer comprises tungsten,  
2 tantalum, or titanium.

1 35. The method as recited in claim 33, wherein said second gate layer comprises a  
2 silicide.

1 36. The method as recited in claim 22, wherein said first reaction product comprises  
2 silicon dioxide.

1 37. The method as recited in claim 22, wherein said first reaction product comprises a  
2 silicide.

1 38. The method as recited in claim 22, wherein said second gate layer comprises a  
2 silicide.

1 39. The method as recited in claim 22, further comprising the steps of  
2 providing metal along sidewalls of said gate conductor; and  
3 recess etching said metal.

1 40. The method as recited in claim 39, wherein the step of chemically reacting further  
2 includes the step of:  
3 reacting said gate conductor with said metal to form a silicide along edges of said  
4 gate conductor adjacent said gate dielectric.

1 41. The method of claim 40, wherein the step of selectively removing said first reaction  
2 product further includes:  
3 etching away said silicide.

1 42. The method of claim 40, wherein said silicide formed along edges of said gate  
2 conductor adjacent said gate dielectric is cobalt silicide, or titanium silicide.

1 43. The method of claim 42, wherein the step of selectively removing said cobalt silicide  
2 or said titanium silicide includes using an hydrogen peroxide mixture, or a hot  
3 sulfuric/hydrogen peroxide mixture.

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